Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-16 (Cancelled).

Claim 17 (Previously Presented): A microprocessor that operates in a manner that conserves power, the microprocessor comprising:

an instruction register for temporarily storing a next instruction to be executed;

an instruction evaluation unit that is connected to said instruction register such that said instruction evaluation unit receives said next instruction from said instruction register, said instruction evaluation unit being configured to evaluate said next instruction in order to produce activity indicators by reading an operation type from the instruction and providing an associated signal comprising one of a clock marker or a no-clock marker based upon the operation types of said instructions;

a functional unit for executing instructions, said functional unit having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator, where said stages of said functional unit are arranged in series;

a memory unit for receiving and registering outputs from the functional unit wherein the amount of time required to register an output from the functional unit comprises time T_r;

a stage activation controller that is connected to said instruction evaluation unit and includes logic gates that utilize said activity indicators in conjunction with a stage activation controller clock pulse C_{SR} to determine which of said stages are to be activated or deactivated and wherein the signal comprising one of a clock marker or a no-clock marker is advanced through a shift register of the stage activation controller such that it takes time T_s to advance each signal comprising one of a clock marker or a no-clock marker a shift register in the stage activation controller;

a clock circuit that supplies the stage activation controller clock pulse C_{SR} to said stage activation controller and also provides a functional unit clock pulse C_{FU} to said functional unit wherein the clock pulse C_{FU} is subject to a gate delay of time T_g, and wherein said functional unit

clock pulse C_{FU} is time-delayed with respect to said stage activation controller clock pulse C_{SR} by an amount of time greater than the sum of times T_s, T_r, and T_g thereby enabling the respective stage of the functional unit to have its power status adjusted depending the requirements of the instruction entering said respective stage of the functional unit.

Claim 18 (Original): A microprocessor as recited in claim 17 wherein the microprocessor is a very long instruction word processor.

Claim 19 (Previously Presented): A microprocessor as recited in claim 17 wherein each of said stages have separate inputs for receiving current, the inputs capable of being separately opened or closed, the activated stages having opened inputs and the deactivated inputs having closed inputs.

Claim 20 (Original): A microprocessor as recited in claim 17 wherein the stage activation controller is a memory unit that stores said activity indicators.

Claim 21 (Original): A microprocessor as recited in claim 20 wherein said memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location storing a respective activity indicator which indicates whether to activate or deactivate a respective stage.

Claim 22 (Original): A microprocessor as recited in claim 17 further comprising a plurality of functional units, each of said functional units having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator.

Claim 23 (Original): A microprocessor as recited in claim 22 further comprising a plurality of stage activation controllers, each of said stage activation controllers using said activity indicators to individually activate or deactivate each of said stages of a respective one of the plurality of functional units.

Claim 24 (Original): A microprocessor as recited in claim 23 further comprising a plurality of instruction evaluation units, each of said instruction evaluation units associated with a respective one of said stage activation controllers.

Claim 25 (Previously Presented): A microprocessor as recited in claim 17 wherein the logic gates of the stage activation controller comprise AND type gates.

Claims 26-39 (Cancelled).